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Digital Object Identifier 10.1109/ACSSC.1999.832397

AbstractPlus | References | Full Text: PDF(212 KB) | IEEE JNL Rights and Permissions 6. A 3.3-V 12-b 50-MS/s A/D converter in 0.6-µm CMOS with over 80-dB SFDR Hui Pan; Segami, M.; Choi, M.; Ling Cao; Abidi, A.A.; Solid-State Circuits, IEEE Journal of Volume 35, Issue 12, Dec. 2000 Page(s):1769 - 1780 Digital Object Identifier 10.1109/4.890290 AbstractPlus | References | Full Text: PDE(340 KB) | IEEE JNL Rights and Permissions 7. A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input Yang, W.; Kelly, D.; Mehr, L.; Sayuk, M.T.; Singer, L.; Solid-State Circuits, IEEE Journal of Volume 36, Issue 12, Dec. 2001 Page(s):1931 - 1936 Digital Object Identifier 10.1109/4.972143 AbstractPlus | References | Full Text: PDF(117 KB) #EEH JNL Rights and Permissions 8. A multichannel pipeline analog-to-digital converter for an integrated 3-D ultrasound imaging _ Kaviani, K.; Oralkan, O.; Khuri-Yakub, P.; Wooley, B.A.; Solid-State Circuits, IEEE Journal of Volume 38, Issue 7, July 2003 Page(s):1266 - 1270 Digital Object Identifier 10.1109/JSSC.2003.813294 AbstractPlus | References | Full Text: PDE(408 KB) | IEEE J&I. Rights and Permissions 9. Digital background calibration of an algorithmic analog-to-digital converter using a simplifie Blecker, E.B.; McDonald, T.M.; Erdogan, O.E.; Hurst, P.J.; Lewis, S.H.; Solid-State Circuits, IEEE Journal of Volume 38, Issue 6, June 2003 Page(s):1059 - 1062 Digital Object Identifier 10.1109/JSSC.2003.811990 AbstractPlus | References | Full Text: PDF(413 KB) IEEE JNL Rights and Permissions 10. A 10-b 30-MS/s low-power pipelined CMOS A/D converter using a pseudodifferential architec Miyazaki, D.; Kawahito, S.; Furuta, M.; Solid-State Circuits, IEEE Journal of Volume 38, Issue 2, Feb. 2003 Page(s):369 - 373 Digital Object Identifier 10.1109/JSSC.2002.807400 AbstractPlus | References | Full Text: PDF(391 KB) :EEE JNL Rights and Permissions 11. A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR Yun Chiu; Gray, P.R.; Nikolic, B.; Solid-State Circuits, IEEE Journal of Volume 39, Issue 12, Dec. 2004 Page(s):2139 - 2151 Digital Object Identifier 10.1109/JSSC.2004.836232 AbstractPlus | References | Full Text: PDF(1040 KB) | IEEE JNL Rights and Permissions 12. A 150-MS/s 8-b 71-mW CMOS time-interleaved ADC Limotyrakis, S.; Kulchycki, S.D.; Su, D.K.; Wooley, B.A.; Solid-State Circuits, IEEE Journal of Volume 40, Issue 5, May 2005 Page(s):1057 - 1067 Digital Object Identifier 10.1109/JSSC.2005.845992 AbstractPlus | References | Full Text: PDF(920 KB) : EEE JNL

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13. A Low Power ROM-Less Direct Digital Frequency Synthesizer with Preset Value Pipelined And Jun Chen; Rong Luo; Huazhong Yang; Hui Wang; VLSi Design, 2006. Held iointty with 5th International Conference on Embedded Systems and Desi Conference on 03-07 Jan. 2006 Page(s):377 - 380 Digital Object Identifier 10.1109/VLSID.2006.15
AbstractPlus Full Text: PDF(288 KB)
14. Clockless Pipelining for Coarse Grain Datapaths Alsharqawi, A.; Ejnioui, A.; VLSi Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Desi Conference on 03-07 Jan. 2006 Page(s):749 - 753 Digital Object Identifier 10.1109/VLSID.2006.60 AbstractPlus Full Text: PDE(272 KB)
15. Modularized pipeline readout electronics for SuperKEKB Higuchi, T.; Hazumi, M.; Ikeno, M.; Itoh, R.; Iwasaki, Y.; Nakao, M.; Nakayoshi, K.; Suzuki, S.Y.; Ta Aulchenko, V.; Bukin, M.A.; Schwartz, B.; Usov, Y.; Wei, B.; Varner, G.S.; Kawasaki, T.; Nakano, F Natkaniec, Z.; Nuclear Science Symposium Conference Record, 2004 IEEE Volume 3, 16-22 Oct. 2004 Page(s):1980 - 1983 Vol. 3 Digital Object Identifier 10.1109/NSSMIC.2004.1462634 AbstractPlus Full Text: PDE(1123 KB) IEEE CNF Rights and Permissions
16. A low-power 4-b 2.5 Gsample/s pipelined flash analog-to-digital converter using differential of DCVSPG encoder Radhakrishnan, S.; Wang, M.; Chen, CI.H.; Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):6142 - 6145 Vol. 6 Digital Object Identifier 10.1109/ISCAS.2005.1466042 AbstractPlus Full Text: PDF(240 KB)
17. A 12-bit, 50 MS/s SiGe BICMOS sample-and-hold residue amplifier Devarajan, S.; Gutmann, R.J.; Rose, K.; Electrical and Computer Engineering, 2004. Canadian Conference on Volume 3, 2-5 May 2004 Page(s):1293 - 1296 Vol.3 AbstractPlus Full Text: PDF(507 KB)
18. Resonant tunnelling diode based QMOS edge triggered flip-flop design Hui Zhang; Mazumder, P.; Kyounghoon Yang; Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 3, 23-26 May 2004 Page(s):III - 705-8 Vol.3 AbstractPlus Full Text: PDF(306 KB) INSEC ONF Rights and Permissions
19. A CMOS low-power ADC for DVB-T and DVB-H systems Adeniran, O.A.; Demosthenous, A.; Clifton, C.; Atungsiri, S.; Soin, R.; Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I-209 - I-212 Vol.1 AbstractPlus Full Text: PDE(276 KB) IEEE CNF
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20. A novel queuing architecture for background calibration of pipeline ADCs Savla, A.; Leonard, J.; Ravindran, A.; <u>Orouits and Systems. 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I-65 - I-68 Vol.1 AbstractPlus Full Text: <u>PDF(252 KB)</u> IIIEE CNII Rights and Permissions</u>
21. A 28mW 10b 80MS/s pipelined ADC in 0.13/spl mu/m CMOS Bogner, P.; Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I - 17-20 Vol.1 Digital Object Identifier 10.1109/ISCAS.2004.1328120 AbstractPlus Full Text: PDE(344 KB) (SIBB CNF) Rights and Permissions
22. Digital error correction and calibration of gain non-linearities in a pipelined ADC Ravindran, A.; Savia, A.; Leonard, J.; Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I-1 - I-4 Vol. 1 Digital Object Identifier 10.1109/ISCAS.2004.1328116 AbstractPlus Full Text: PDF(395 KB) ISSE CNF Rights and Permissions
23. An IF-sampling timing skew-insensitive parallel S/H circuit Aho, M.; Hakkarainen, V.; Sumanen, L.; Waltari, M.; Halonen, K.; Circuits and Systems, 2004, ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I - 1052-5 Vol.1 Digital Object Identifier 10.1109/ISCAS.2004.1328379 AbstractPlus Full Text: PDF(256 KB) ISEES CNF Rights and Permissions
24. Multi-GHz systems clocking Oklobdzija, V.G.; ASIC, 2003. Proceedings. 5th International Conference on Volume 2, 21-24 Oct. 2003 Page(s):701 - 706 Vol.2 AbstractPlus Full Text: PDF(436 KB) ISSES CNF Rights and Permissions
25. A low-power 6-b integrating-pipeline hybrid analog-to-digital converter [Bluetooth transceive Diduck, Q.; Margala, M.; SOC Conference, 2003, Proceedings, IEEE International [Systems-on-Chip] 17-20 Sept. 2003 Page(s):337 - 340 Digital Object Identifier 10.1109/SOC.2003.1241538 AbstractPlus Full Text: PDF(338 KB) IEEE CNF Rights and Permissions

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		П	2.	A 10 b 50 MHz pipelined CMC Yotsuyanagi, M.; Etoh, T.; Hirat Solid-Slate Circuits, JEEE, Journ Volume 28, Issue 3, March 19 Digital Object Identifier 10.1109 AbstractPlus Full Text: PDE(7 Rights and Permissions	a, K.; nai.of 93 Page(s):292 - 300 0/4.209996	n S/H		
			3.	A CMOS transistor-only 8-b 4 circuit techniques Chung-Yu Wu; Chih-Cheng Ch Solid-State Circuits, IEEE Journ Volume 30, Issue 5, May 1999 Digital Object Identifier 10.1109 AbstractPlus Full Text: PDE(9) Rights and Permissions	en; Jyh-Jer Cho; nai of Page(s):522 - 532 //4.384165	alog-to-digital converter using	g fully-differe	
		n	4.	A 10-b 20-Msample/s low-pov Won-Chul Song; Hae-Wook Ch Solid-State Circuits, IEEE Journ Volume 30, Issue 5, May 1999 Digital Object Identifier 10.1109 AbstractPlus Full Text: PDE(6 Rights and Permissions	oi; Sung-Ung Kwak; E nal.of 5 Page(s):514 - 521 0/4.384164	ang-Sup Song;		

Volume 35, Issue 12, Dec. 2000 Page(s):1781 - 1790 Digital Object Identifier 10.1109/4.890291

Myung-Jun Choe; Bang-Sup Song; Bacrania, K.;

Solid-State Circuits, IEEE Journal of

5. A 13-b 40-MSamples/s CMOS pipelined folding ADC with background offset trimming

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AbstractPlus | Full Text: PDF(348 KB) ISEE CNF Rights and Permissions 31. An experimental low-power CMOS pipeline ADC using feedforward sample-and-hold amplific Chi-Tat Tam; Elmasry, M.I.; Electrical and Computer Engineering, 1998, IEEE Canadian Conference on Volume 1, 24-28 May 1998 Page(s):257 - 260 vol.1 Digital Object Identifier 10.1109/CCECE.1998.682731 AbstractPlus | Full Text: PDF(336 KB) IEEE CNF Rights and Permissions 32. A 14-bit 10-MHz calibration-free CMOS pipelined A/D converter Singer, L.A.; Brooks, T.L.; VLSi Circuits, 1996. Digest of Technical Papers, 1996 Symposium on 13-15 June 1996 Page(s):94 - 95 Digital Object Identifier 10.1109/VLSIC.1996.507727 AbstractPlus | Full Text: PDF(160 KB) | III EE CNF Rights and Permissions

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